1. Specifications:

Model	MMP5000B5-16G
GPU Architecture	NVIDIA Pascal
Graphics Processing Unit	NVIDIA Quadro P5000m
NVIDIA CUDA Core	2048
Bus Type	MXM3 .1 / up to PCI Express 3.0
Graphics Clock	1278MHz / 1582MHz (Boost)
Memory Clock	1502MHz (6.0 Gbps)
Memory Bandwidth	192.3 GB/s
Single Precision FLOPS	6494GFLOPS
Double Precision FLOPS	209.1GFLOPS
Memory Size	16G 256bit GDDR5
Display Features	DP_A: Display Port1.4++ DP_B: Display Port1.4++ DP_C: Display Port1.4++ DP_D: Display Port1.4++
Max Resolution	7680x4320@120Hz
Board Power	112W (Option 97W)
Board Dimensions	MXM Graphics Module Version 3.1 Type B (105x82mm)
Number of output Channel	4
Operation System	Windows 7/8/8.1/10 64bit、Linux 64bit
VIN Range	DC 12~19V, 3.3V & 5V; +/-5%

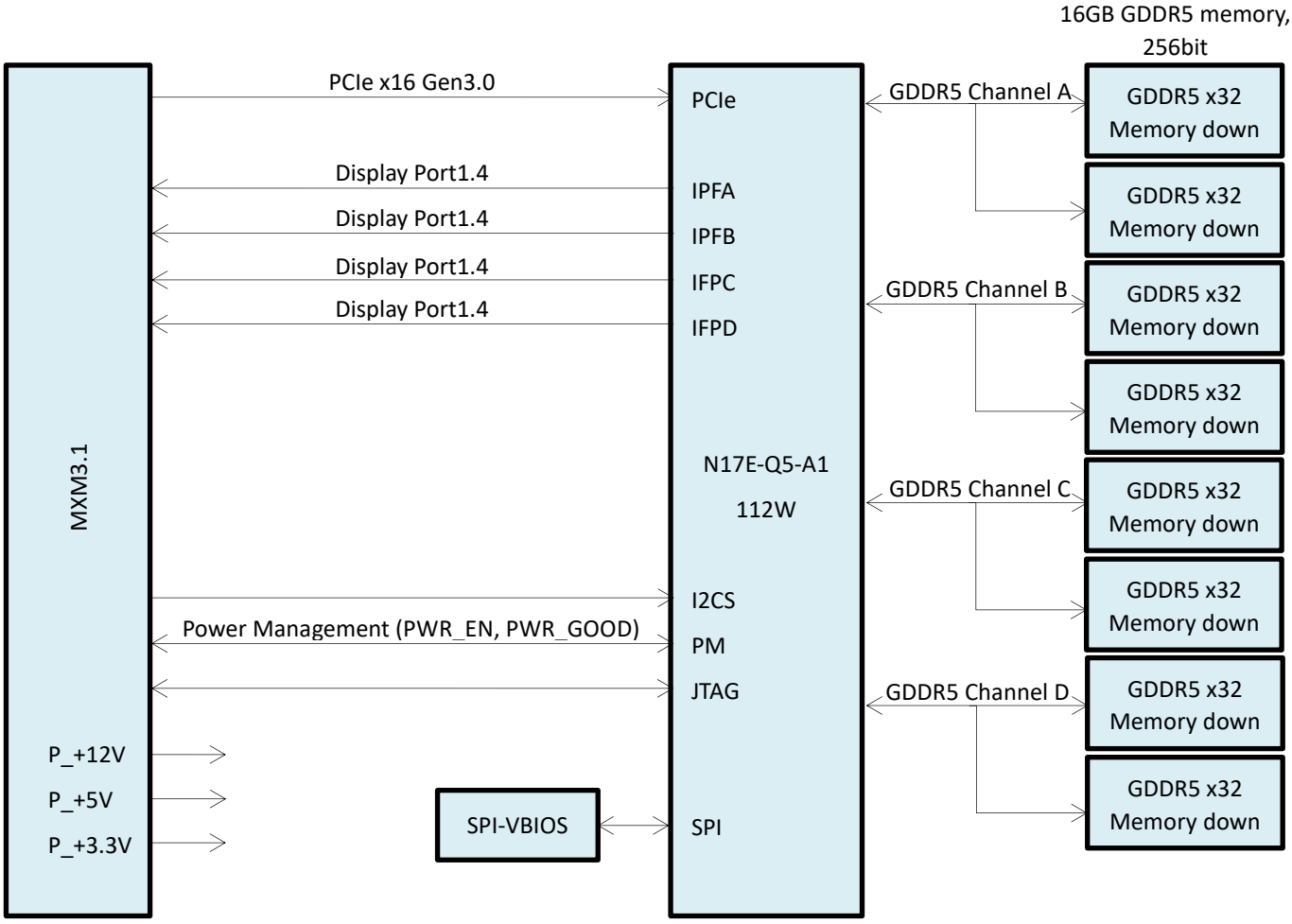
OpenGL	4.6
OpenCL	1.2
DirectX	12
Video Playback	H.265, VC1, MPEG2 1080P

Operating Temperature	0~45°C (Option -20°C)
Storage Temperature	-20~75°C
Operating Humidity	0~95% (non-condensing)
Storage Humidity	10~90%

Surround (Landscape)	**Surround (Portrait)**
2x1(3840x1080@60Hz)	2x1(2160x1920@60Hz)
1x2(1920x2160@60Hz)	1x2(1080x3840@60Hz)
3x1(5760x1080@60Hz)	3x1(3240x1920@60Hz)
1x3(1920x3240@60Hz)	1x3(1080x5760@60Hz)
4x1(7680x1080@60Hz)	4x1(1080x7680@60Hz)
1x4(7680x1080@60Hz)	1x4(1080x7680@60Hz)
2x2(3840x2160@60Hz)	2x2(2160x3840@60Hz)

**Total resolution based on every display resolution is 1920*1080@60Hz.*

2.Block Diagram:



3.MXM Board Outlines:

Figure 3.1 shows the board outlines (top side view) for Type B MXM modules. An additional system keep-out of 0.5mm[0.020] per side is allowed on the PCB to accommodate whatever means of production panelization is required. This additional clearance is above and beyond the dimensional limits presented here. The location of these features is not specified or controlled.

Figure 3.1: Board Outlines

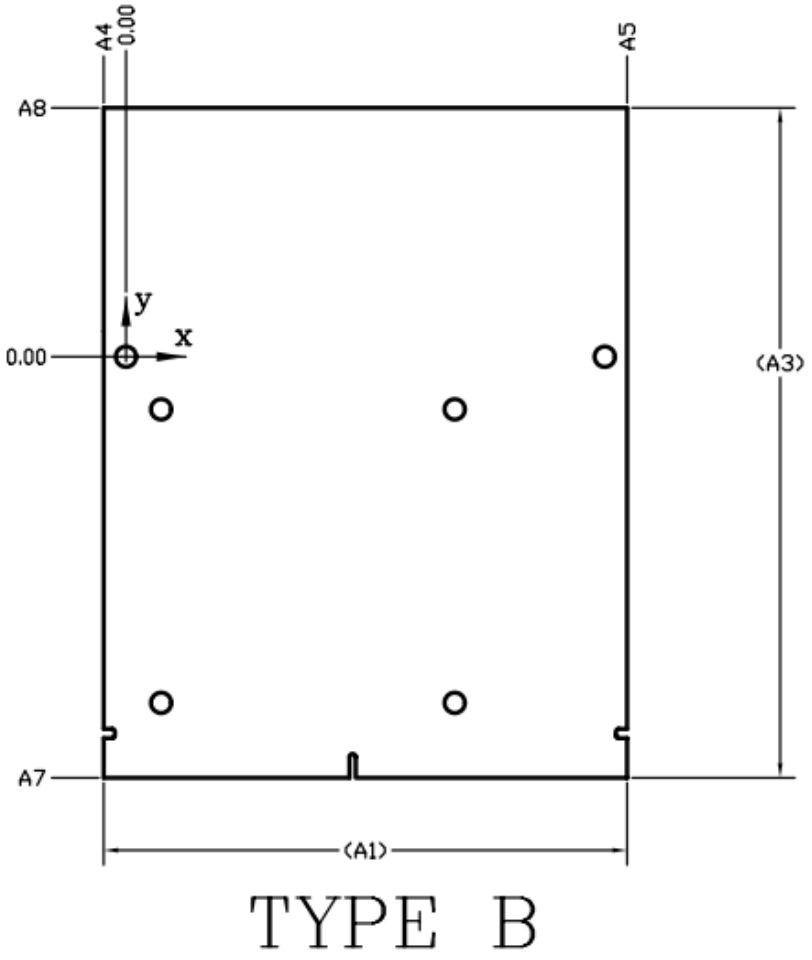


Table 3.1: Board Outline Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A1		82.00			3.228	
A3		105.00			4.134	
A4	3.37	3.50	3.63	0.133	0.138	0.143
A5	78.37	78.50	78.63	3.085	3.091	3.096
A7	65.87	66.00	66.13	2.593	2.598	2.604
A8	38.87	39.00	39.13	1.530	1.535	1.541

Figure 3.2: Board Slots Detail

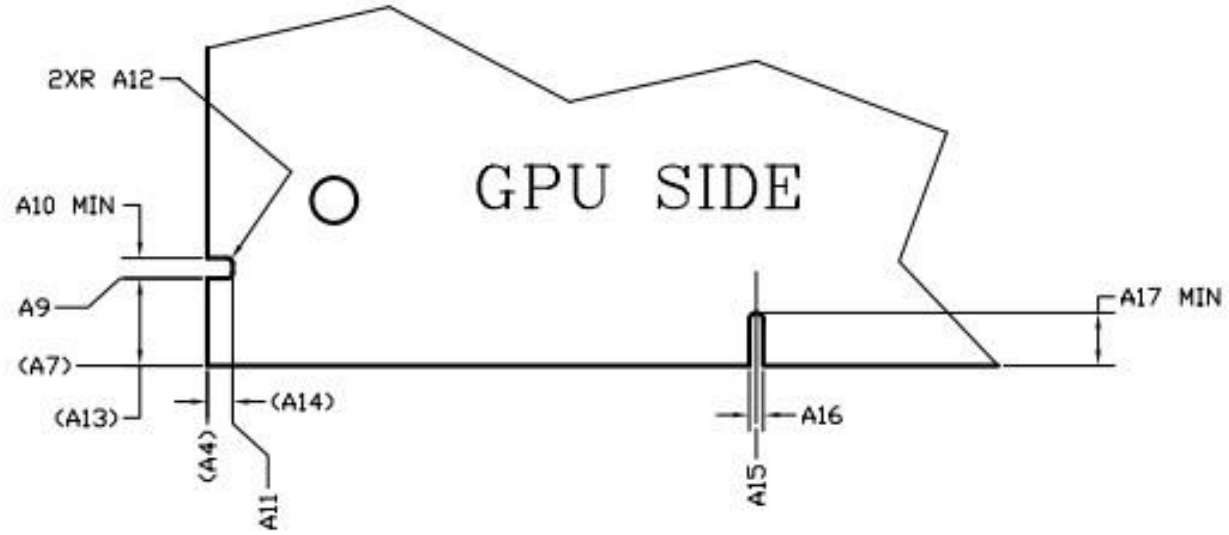


Table 3.2: Board Slots Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
A4		3.50			0.138	
A7		66.00			2.598	
A9	59.67	59.80	59.93	2.349	2.354	2.359
A10	1.45			0.057		
A11	1.57	1.70	1.83	0.062	0.067	0.072
A12	0.32	0.50	0.58	0.013	0.020	0.023
A13		6.20			0.244	
A14		1.80			0.071	
A15	35.37	35.50	35.63	1.393	1.398	1.403
A16	0.95	1.00	1.05	0.037	0.039	0.041
A17	3.75			0.148		

4.MXM PCB Mounting Holes:

All MXM version 3.1 modules have 6 holes. Two are used to secure the board to the system and the other four to fasten the thermal solution to the module.

Figure 4.1: Mounting Holes

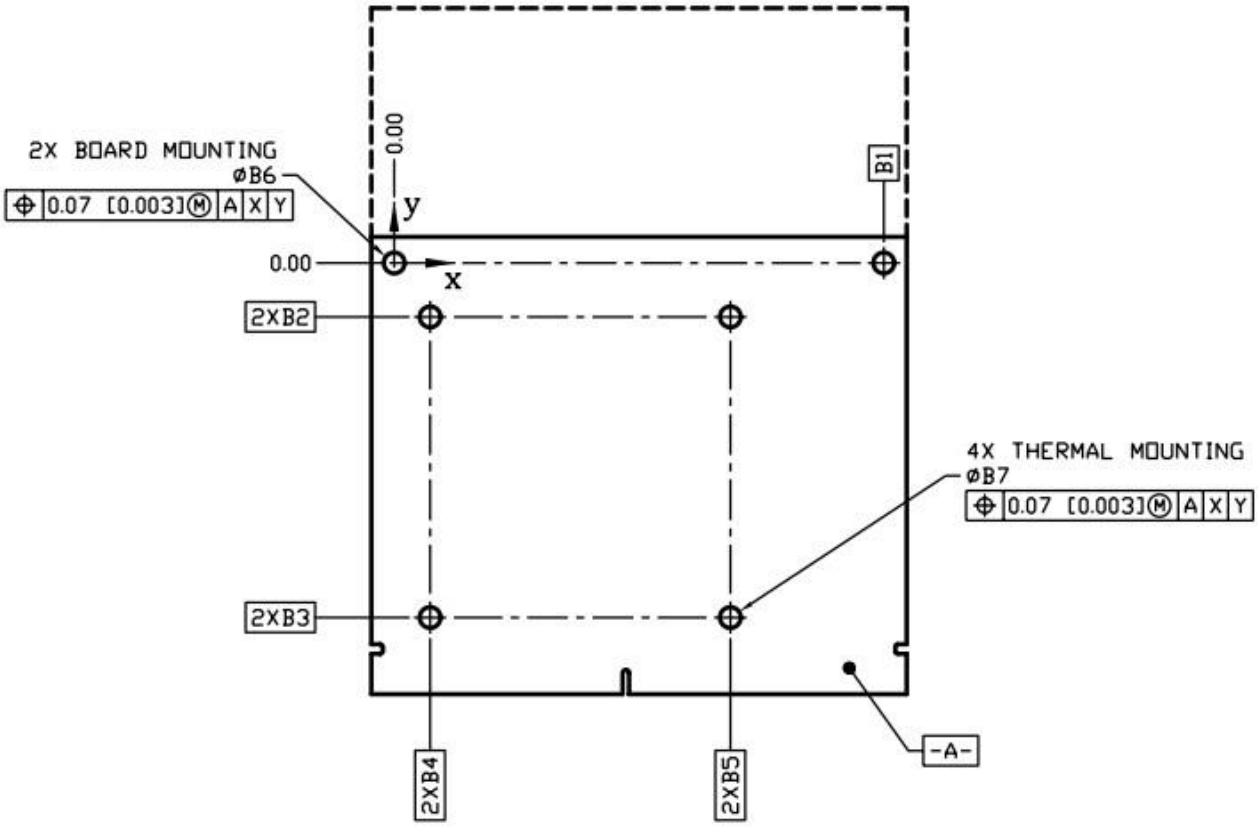


Table 4.1: Mounting Holes Dimensions

Symbol	[mm]			[in]		
	min	nom	max	min	nom	max
B1		75.00			2.953	
B2		8.25			0.325	
B3		54.25			2.136	
B4		5.50			0.217	
B5		51.50			2.028	
B6	3.07	3.20	3.33	0.121	0.126	0.131
B7	3.07	3.20	3.33	0.121	0.126	0.131

5.Connector Pinout:

Table 5.1, Table 5.2 and Table 5.3 list the connector pinout.

Table 5.1: Connector Pinout

Pin	Signal Name	Pin	Signal Name
E1	PWR_SRC	E2	PWR_SRC
E3	GND	E4	GND
1	5V	2	PRSNT_R
3	5V	4	WAKE
5	5V	6	PWR_GOOD
7	5V	8	PWR_EN
9	5V	10	27MHZ_REF
11	GND	12	GND
13	GND	14	LVDS_U_HPD DP_F_HPD
15	GND	16	RSVD
17	GND	18	PWR_LEVEL
19	PEX_STD_SW#	20	TH_OVERT#
21	VGA_DISABLE#	22	TH_ALERT#
23	N/A	24	TH_PWM
25	N/A	26	GPIO0
27	N/A	28	GPIO1
29	HDMI_CEC	30	GPIO2
31	LVDS_L_HPD DP_E_HPD	32	SMB_DAT
33	LVDS_DDC_DAT NC	34	SMB_CLK
35	LVDS_DDC_CLK NC	36	GND
37	GND	38	OEM0
39	OEM1	40	OEM2
41	OEM3	42	OEM4
43	OEM5	44	OEM6
45	OEM7	46	GND
47	GND	48	PEX_TX15#
49	PEX_RX15#	50	PEX_TX15

Pin	Signal Name	Pin	Signal Name
51	PEX_RX15	52	GND
53	GND	54	PEX_TX14#
55	PEX_RX14#	56	PEX_TX14
57	PEX_RX14	58	GND
59	GND	60	PEX_TX13#
61	PEX_RX13#	62	PEX_TX13
63	PEX_RX13	64	GND
65	GND	66	PEX_TX12#
67	PEX_RX12#	68	PEX_TX12
69	PEX_RX12	70	GND
71	GND	72	PEX_TX11#
73	PEX_RX11#	74	PEX_TX11
75	PEX_RX11	76	GND
77	GND	78	PEX_TX10#
79	PEX_RX10#	80	PEX_TX10
81	PEX_RX10	82	GND
83	GND	84	PEX_TX9#
85	PEX_RX9#	86	PEX_TX9
87	PEX_RX9	88	GND
89	GND	90	PEX_TX8#
91	PEX_RX8#	92	PEX_TX8
93	PEX_RX8	94	GND
95	GND	96	PEX_TX7#
97	PEX_RX7#	98	PEX_TX7
99	PEX_RX7	100	GND
101	GND	102	PEX_TX6#
103	PEX_RX6#	104	PEX_TX6

Table 5.2: Connector Pinout(continued)

Pin	Signal Name	Pin	Signal Name
105	PEX_RX6	106	GND
107	GND	108	PEX_TX5#
109	PEX_RX5#	110	PEX_TX5
111	PEX_RX5	112	GND
113	GND	114	PEX_TX4#
115	PEX_RX4#	116	PEX_TX4
117	PEX_RX4	118	GND
119	GND	120	PEX_TX3#
121	PEX_RX3#	122	PEX_TX3
123	PEX_RX3	124	GND
125	GND	126	KEY
127	KEY	128	KEY
129	KEY	130	KEY
131	KEY	132	KEY
133	GND	134	GND
135	PEX_RX2#	136	PEX_TX2#
137	PEX_RX2	138	PEX_TX2
139	GND	140	GND
141	PEX_RX1#	142	PEX_TX1#
143	PEX_RX1	144	PEX_TX1
145	GND	146	GND
147	PEX_RX0#	148	PEX_TX0#
149	REX_RX0	150	PEX_TX0
151	GND	152	GND

Pin	Signal Name	Pin	Signal Name
153	PEX_REFCLK#	154	PEX_CLK_REQ#
155	PEX_REFCLK	156	PEX_RST#
157	GND	158	N/A
159	JTAG_TDO	160	N/A
161	JTAG_TDI	162	N/A
163	JTAG_TCLK	164	N/A
165	JTAG_TMS	166	GND
167	JTAG_TRST#	168	N/A
169	DP_F_L3 LVDS_UCLK#	170	N/A
171	DP_F_L3 LVDS_UCLK	172	N/A
173	GND	174	GND
175	DP_F_AUX LVDS_UTX3#	176	DP_E_L3 LVDS_LCLK#
177	DP_F_AUX LVDS_UTX3	178	DP_E_L3 LVDS_LCLK
179	GND	180	GND
181	DP_F_L0 LVDS_UTX2#	182	DP_E_AUX LVDS_LTX3#
183	DP_F_L0 LVDS_UTX2	184	DP_E_AUX LVDS_LTX3
185	GND	186	GND
187	DP_F_L1 LVDS_UTX1#	188	DP_E_L0 LVDS_LTX2#
189	DP_F_L1 LVDS_UTX1	190	DP_E_L0 LVDS_LTX2
191	GND	192	GND
193	DP_F_L2 LVDS_UTX0#	194	DP_E_L1 LVDS_LTX1#
195	DP_F_L2 LVDS_UTX0	196	DP_E_L1 LVDS_LTX1
197	GND	198	GND
199	DP_C_L0#	200	DP_E_L2 LVDS_LTX0#

Table 5.3: Connector Pinout(continued)

Pin	Signal Name	Pin	Signal Name
201	DP_C_L0	202	DP_E_L2 LVDS_LTX0
203	GND	204	GND
205	DP_C_L1#	206	DP_D_L0#
207	DP_C_L1	208	DP_D_L0
209	GND	210	GND
211	DP_C_L2#	212	DP_D_L1#
213	DP_C_L2	214	DP_D_L1
215	GND	216	GND
217	DP_C_L3#	218	DP_D_L2#
219	DP_C_L3	220	DP_D_L2
221	GND	222	GND
223	DP_C_AUX#	224	DP_D_L3#
225	DP_C_AUX	226	DP_D_L3
227	RSVD	228	GND
229	RSVD	230	DP_D_AUX#
231	RSVD	232	DP_D_AUX
233	RSVD	234	DP_C_HPD
235	RSVD	236	DP_D_HPD
237	RSVD	238	RSVD
239	RSVD	240	3V3
241	RSVD	242	3V3

Pin	Signal Name	Pin	Signal Name
243	RSVD	244	GND
245	RSVD	246	DP_B_L0#
247	RSVD	248	DP_B_L0
249	RSVD	250	GND
251	GND	252	DP_B_L1#
253	DP_A_L0#	254	DP_B_L1
255	DP_A_L0	256	GND
257	GND	258	DP_B_L2#
259	DP_A_L1#	260	DP_B_L2
261	DP_A_L1	262	GND
263	GND	264	DP_B_L3#
265	DP_A_L2#	266	DP_B_L3
267	DP_A_L2	268	GND
269	GND	270	DP_B_AUX#
271	DP_A_L3#	272	DP_B_AUX
273	DP_A_L3	274	DP_B_HPD
275	GND	276	DP_A_HPD
277	DP_A_AUX#	278	3V3
279	DP_A_AUX	280	3V3
281	PRSNT_L	-	

6.MXM Connector:

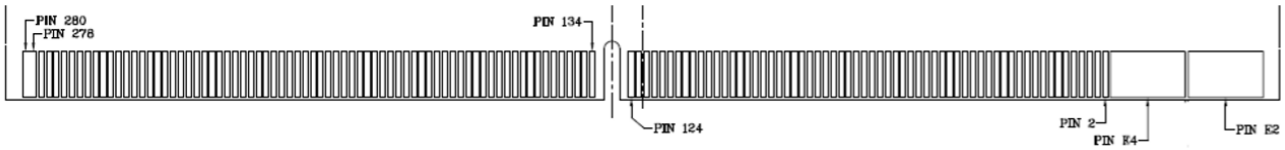


Figure 6.1 MXM Connector (Card Top)

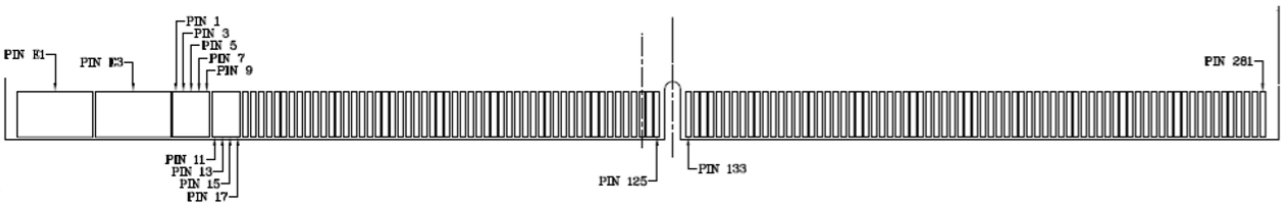


Figure 6.2 MXM Connector (Card Bottom)

7.Power Group:

Table 7.1 shows the MXM module power requirements. The voltage tolerances in the table are specified as measured on module edge finger. The system must be able to supply the full specified current on rails (except PWR_SRC) at all times. Th current capability of the PWR_SRC rail must be defined by the system in the MXM system information structure.

Table 7.1: MXM Power Rails

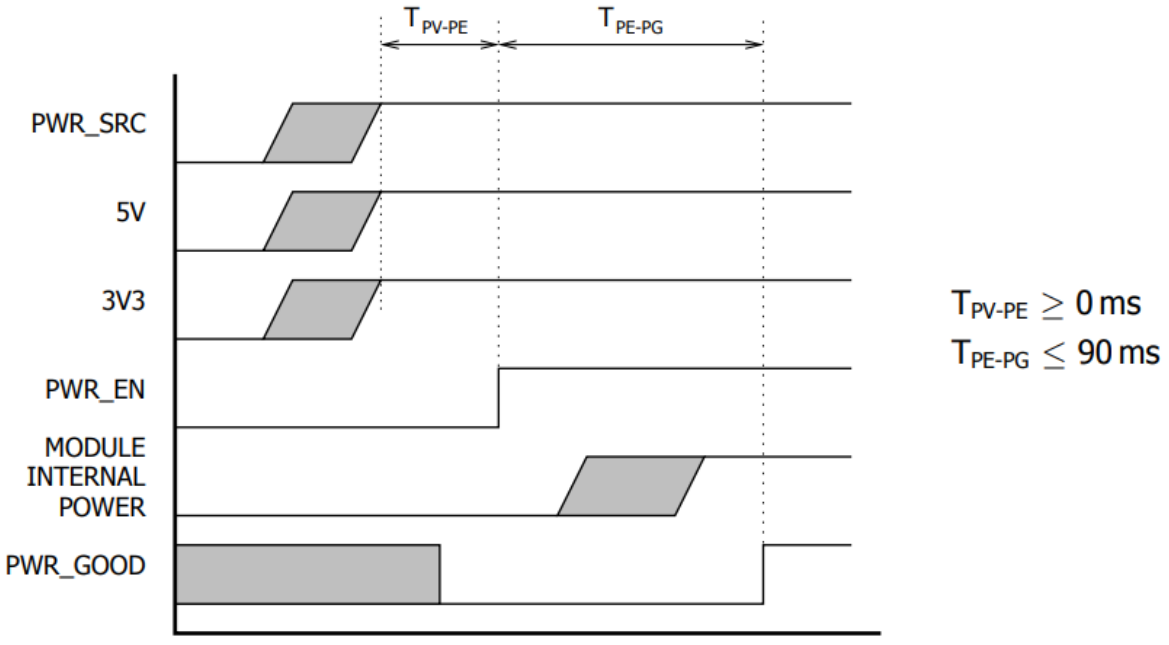
Signal Name	I/O	Type	Impedance	Voltage	Current
PWR_SRC	I	Power	N/A	12-19V	up to 10A
5V	I	Power	N/A	5.0V ± 6%	2.5A
3.3V	I	Power	N/A	3.3V ± 6%	2.0A

Note: PWR_SRC voltage range is assumed to be DC or RMS. However under any circumstances the maximum peak voltage shall not exceed 22V and minimum voltage shall not fall below 6.5V.

8.Power Sequencing:

There is no power sequencing requirement for the input voltages to the MXM module. However the PWR_EN signal may be asserted only after all power rails are within specified tolerance. The state of PWR_GOOD is undefined until all rails are fully ramped. Refer to Figure 8.1 for details

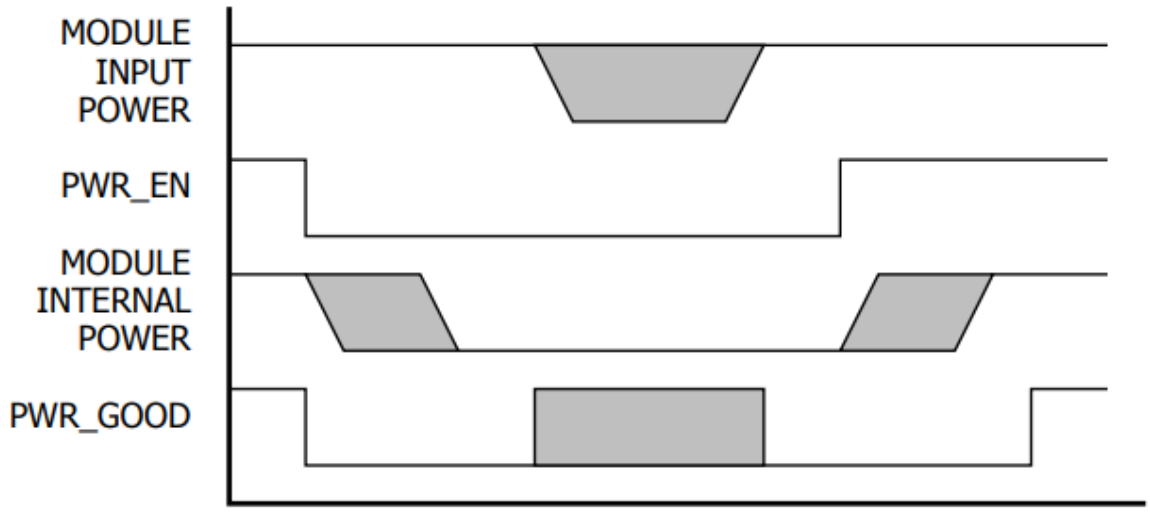
Figure 8.1 Power Sequencing



9.Module Power Down and Power Up:

The MXM module may be powered down using the PWR_EN signal. The system designer may choose to shut down or keep the input power while the module is powered down. Refer to Figure 9.1 for details.

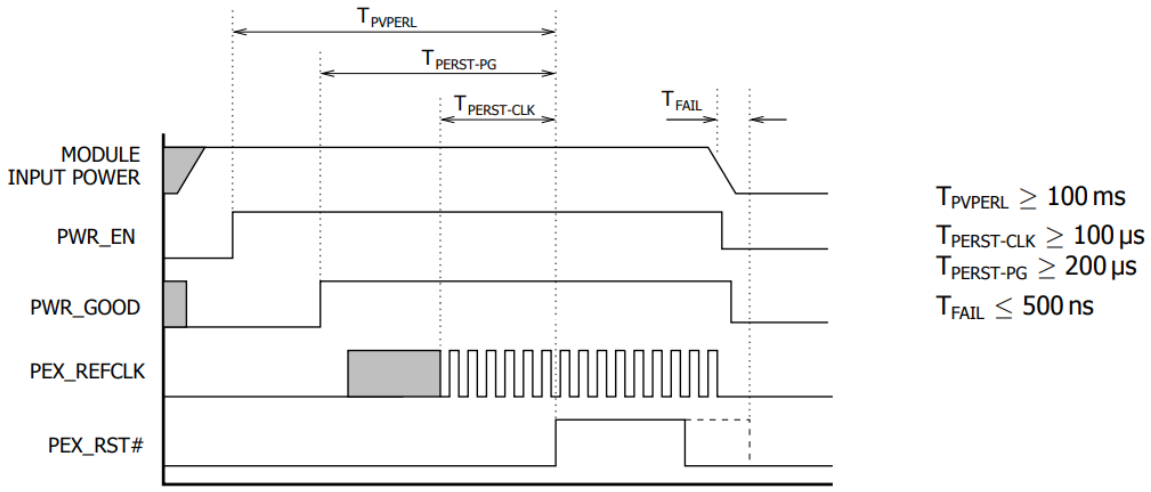
Figure 9.1 Module Power Down



10.Reset Requirements:

System reset may be deasserted only after the assertion of the PWR_GOOD signal. Figure 10.1 shows the reset requirements relative to the PWR_EN and PWR_GOOD signals. This sequence must be followed on initial power on, system reset and resume from suspend/hibernate.

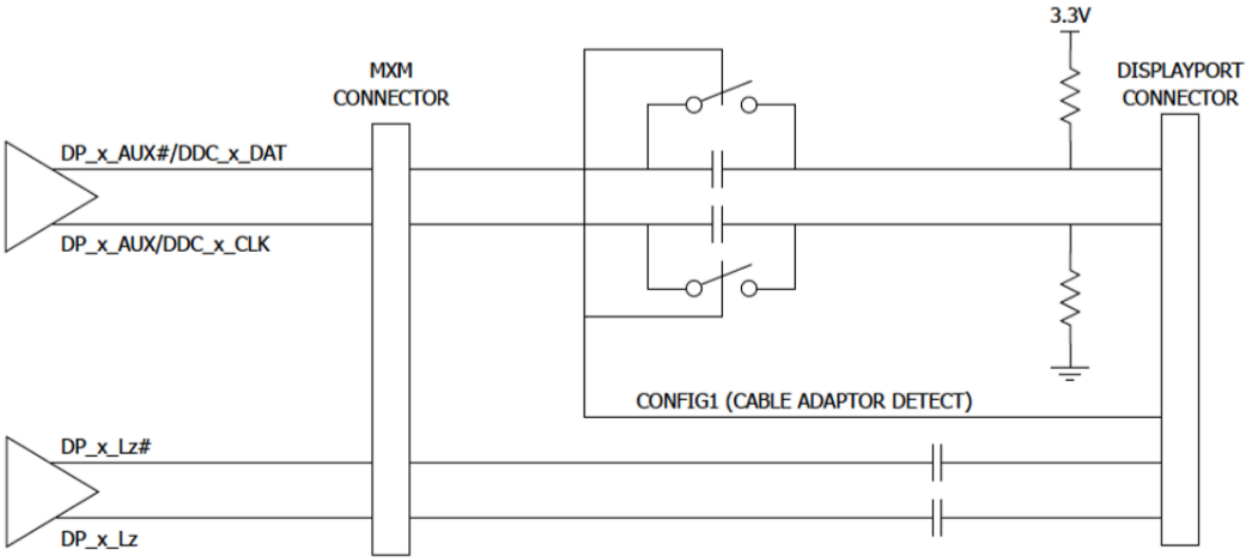
Figure 10.1 Reset Sequencing



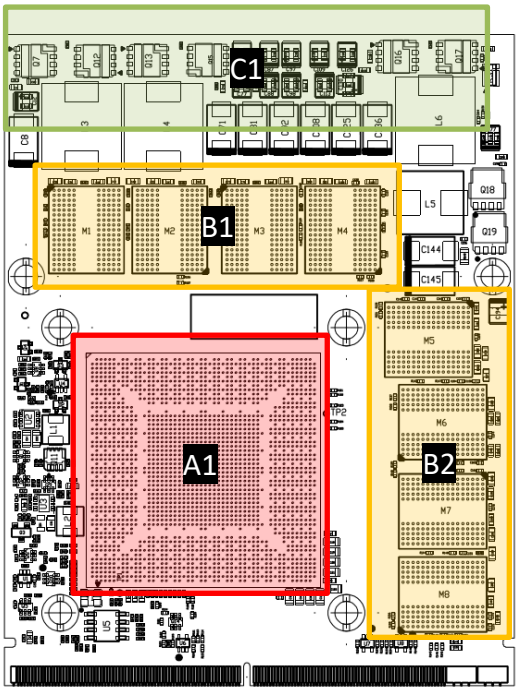
11.DisplayPort Interface:

DC blocking capacitors of DisplayPort must be placed on the system board. In addition to the MXM implementation of Dual-mode DisplayPort requires the circuit in Figure 11.1 on the AUX lines for proper dongle detection. The HPD signal conditioning must also be placed on the system board.

Figure 11.1 Dual-mode DisplayPort Implementation



12.Thermal:



Components	Area	TDP	Height
GPU	A1	87W	2.4mm
Memory	B1	1.5W*4	0.9mm
Memory	B2	1.5W*4	0.9mm
Mosfet	C1	2W*8	0.75mm

Chipset		Specification
Dimensions		16.5*19.5mm
Stress	Maximum	75 PSI
	Normal	30-40 PSI

Cooling Suggestion:

1、显卡建议先固定在散热器上，散热器外径为 4mm，M2 的螺柱。

2、散热器的重量要用箱体来支撑固定。

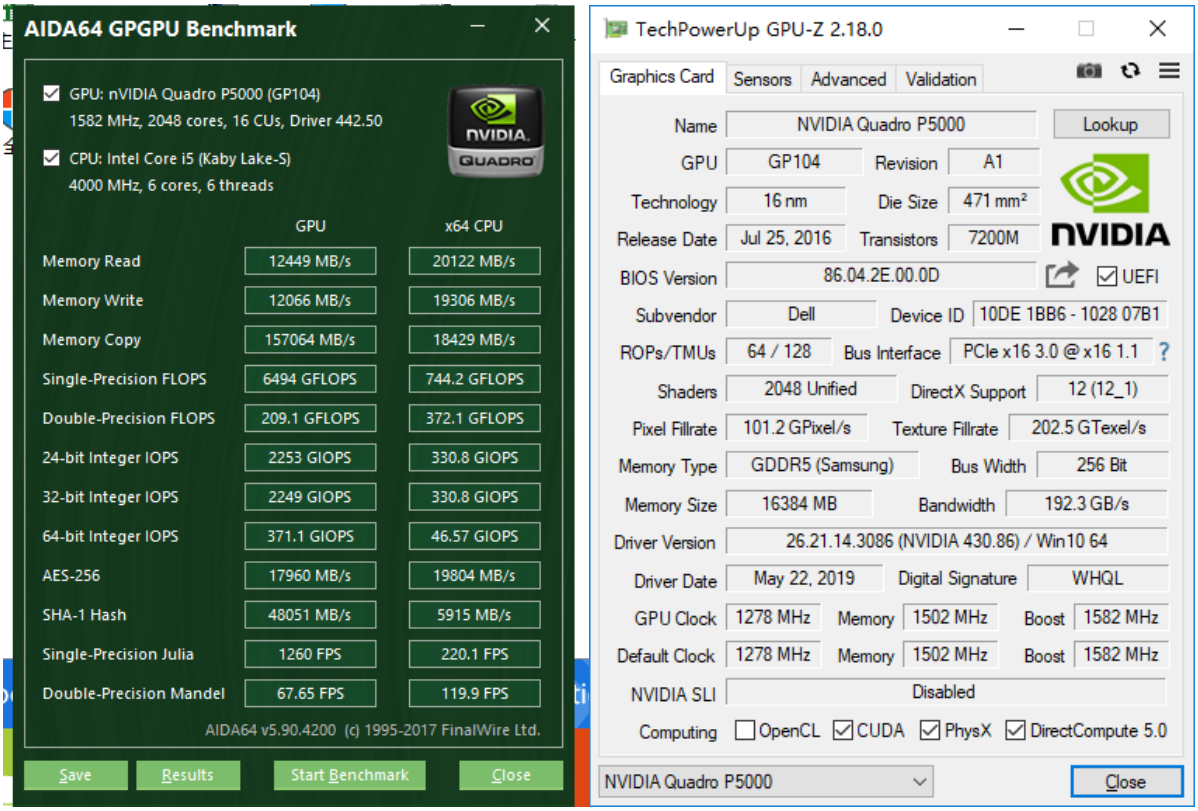
3、显存和 MOS 要加导热垫。

Components	壳温满载限温（环温 45℃）
GPU	95℃
Memory	85℃
Mosfet	105℃

**显存和 MOS 由“探针”监测；GPU 由“Furmark（1920*1080）”监测。*

13.Performance:

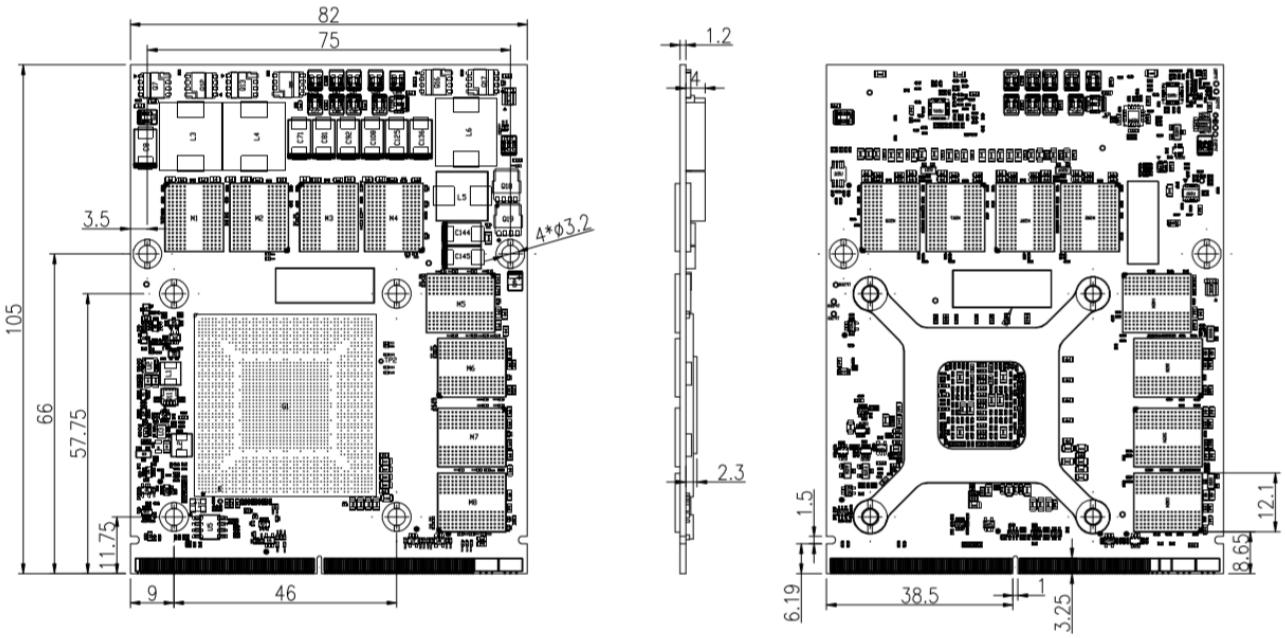
3Dmark13	12720	Cuda	
3Dmark11	P15413 X6876	single kernels	4367.13 / 155.763
3Dmark Vantage	41550	N=10 w/o streams	4915.69 /198.913
Heaven	5630	N=10 with streams	5395.71 / 197.42
鲁大师	199701	N=10 batched	6098.41 / 199.216



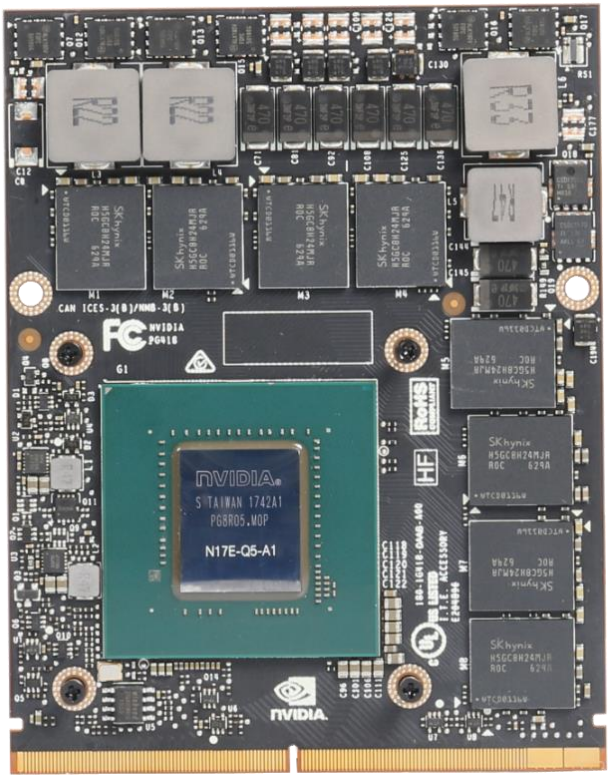
14.Driver:

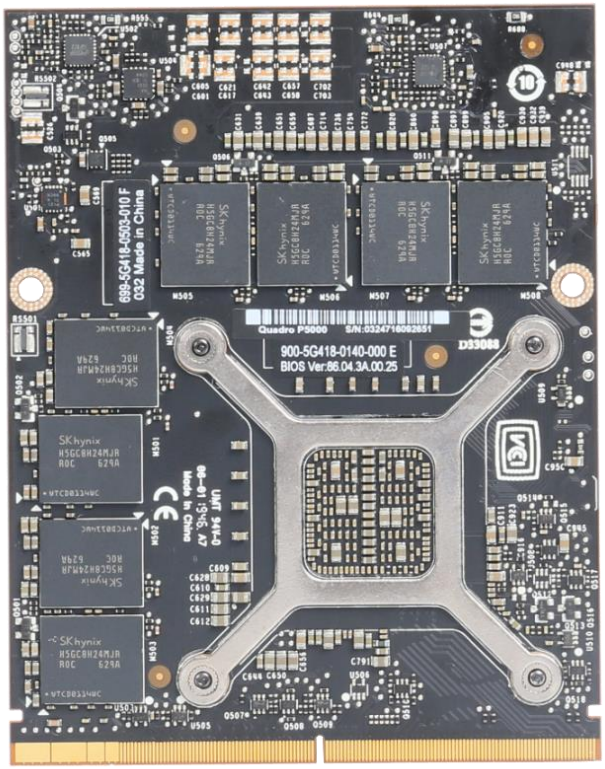
Windows 11: https://pan.baidu.com/s/1yYimF3LHJH9Gh5AgzI9ATQ?pwd=0zbh
Windows 10 64bit: https://pan.baidu.com/s/1yYimF3LHJH9Gh5AgzI9ATQ?pwd=0zbh
Windows 7 64bit: https://pan.baidu.com/s/1sqgegJp__DlBH6EIEerGNQ?pwd=f7gq
Linux 64bit: https://cn.download.nvidia.com/XFree86/Linux-x86_64/450.80.02/NVIDIA-Linux-x86_64-450.80.02.run

15. Dimensions:



16.Photo:





17.Question:

故障	排除
不开机	1、更改 pgood 信号。（部份主板） 2、确认 PCIE 复位信号。 3、主板 BIOS 更改为 UEFI BIOS。
不显示	**Windows 10：**（需 1809 版本之后） 在主板 BIOS 下，将 CSM 中 CSM Support 设置由 Enabled 更改为 Disabled。 **Windows7：** 在主板 BIOS 下，将 CSM 中 CSM Support 设置由 Enabled 更改为 Disabled，并将 Video 设置由 legacy 更改为 UEFI。
不显示（HDMI 输出）	1、4K 60Hz 显示屏，确认 HDMI 线材是否为 HDMI2.0。 2、将显示器分辨率降为 2K 60Hz。
设备管理员出现惊叹号	1、原系统显卡驱动删除干净。（请使用 Display Driver Uninstaller 删除，https://www.wagnardsoft.com/） 2、Windows 10 版本 16299 不支持，需更新至最新版（17763、17134 均可）。 3、Windows 7 打补丁 KB2685811。 4、确认核显驱动是否已安装。（不需独立显卡显示）
显卡不工作	量下 3V3/5V/2V/Reset 信号是否有电/短路？若有电，显卡就会工作。
显卡无法辨视	检查 PCIE LANE Numbering Reversal 设置。
安装 Linux 系统，图形界面异常/无限循环登陆界面，无法登录系统	装驱动的时，加上--no-opengl-files。 （禁用 opengl，若系统上有用到这套组件，将无法使用）
控制面板无法正常开启	仅可在独显显示时，才能正常开启；若使用集显显示，将无法正常开启。
集显及独显在 Win7 下，无法同时开启 3D 启动	打系统补丁（KB2685811），解压后，把所有文件 COPY 到 C 盘 根目录下运行 BAT 文件。
X86 在中标麒麟系统下，显卡驱动后集显输出不能进系统	将 xorg.conf 文件内容清空。

18.Part Number:

Model	Part Number	Specification
MMP5000B5-16G	8.ZRT.80-6427-00-LFF	P5000M 16G 256bit GDDR5 256*32 MXM Type B-工包
MMP5000B5-16G(-20)	8.ZRT.80-6427-03-LFF	P5000m 16G 256bit GDDR5 256*32 Samsung 4DP MXM Type B -20 度-ZRT 彩包二十入